ABSTRACT OF THE DISCLOSURE

Sub-blocks SBA0-SBA3, SBB0-SBB3, SBC0-SBC3, SBD0-SBD3 respectively form four groups. In each group, a refresh end signal REF_END is successively transferred to the next sub-block. Therefore, when a refresh counter of the number of bits corresponding to the number of word lines present in a sub-block is provided in a central control circuit, a memory capacity can easily be redesigned by changing the number of sub-blocks and changing a group configuration of sub-blocks. As a result, there can be provided a memory core for embedded memory in which a memory capacity can easily be changed and a refresh control-related circuitry can easily be changed.